Claims

1. (Previously Presented) An integrated circuit inductor comprising:

a substrate;

a spiral inductor metalization pattern disposed on the substrate including a plurality of parallel tracks in a spiral pattern each track having a first end and a second end and having the first ends coupled together and the second ends coupled together; and

a n+ diffusion layer disposed in the substrate directly underneath the spiral inductor metalization pattern; the n^+ diffusion layer has a fingered pattern shape with n+ fingers electrically isolated by regions of polysilicon.

2. (Previously Presented) The integrated circuit inductor of claim 1, wherein the substrate is fabricated utilizing a CMOS process.

3. (Previously Presented) The integrated circuit inductor of claim 1, wherein the spiral inductor is a square configuration.

4. (Previously Presented) The integrated circuit inductor of claim 1, wherein the spiral inductor is a octagonal configuration.

5. (Previously Presented) The integrated circuit inductor of claim 1, in which the plurality of tracks are disposed in a common layer of the substrate.

6. (Previously Presented) The integrated circuit inductor of claim 1, in which the plurality of tracks are disposed in different layers of the substrate.

7. (Previously Presented) The integrated circuit inductor of claim 1, in which the plurality of tracks are disposed in different layers of the substrate and coupled together with a via.

8-10. (Canceled).

11. (Previously Presented) The integrated circuit inductor of claim 1, in which the fingered pattern is coupled to a common ground reference.

12. (Previously Presented) The integrated circuit inductor of claim 11, in which the n^+ diffusion layer further comprises a second fingered pattern coupled to the common ground reference by a conductive strip that does not provide a ground loop path

13. (Canceled).

14. (Currently Amended) An integrated circuit inductor comprising:

a substrate having a first layer and a second layer;

a first track disposed on the first layer in a first spiral pattern and having a first input and a first output;

a second track disposed on the second layer in a second spiral pattern and having a second input and a second output, the second spiral pattern oriented parallel to the first spiral pattern; and

a pattern of via holes sufficient to couple a varying voltage present along the length of the first track on to the second track;

the first and second inputs connected together by a first via hole of the pattern of via holes, and the first and second outputs connected together by a second via hole of the pattern of via holes[.];

said first track and said second track operating in parallel from said first and second inputs to said first and second outputs.

15-23. (Canceled).

24. (Currently Amended) An integrated circuit inductor, comprising:

a substrate having a first layer and a second layer;

a first spiral pattern disposed on the first layer of the substrate and having a first end and a second end;

a second spiral pattern disposed on the second layer of the substrate and oriented parallel to the first spiral pattern, and having a first end and a second end; and

the first end of the a first spiral pattern connected to the first end of the second spiral pattern and forming an input for the integrated circuit inductor, and the second end of the first spiral pattern connected to the second end of the second spiral pattern and forming an output for the integrated circuit inductor[.]

said first spiral pattern and said second spiral pattern operating in parallel from said input to said output.

25. (Previously Presented) The integrated circuit inductor of claim 24, further comprising a plurality of via holes disposed along a length of the first spiral pattern and connected to the second spiral pattern.

26. (Previously Presented) The integrated circuit inductor of claim 24, further comprising a n+ diffusion layer disposed in the substrate beneath the first spiral pattern and the second spiral pattern.

27. (Previously Presented) The integrated circuit inductor of claim 26, wherein the n+ diffusion layer is formed in a fingered pattern from n+ material having n+ fingers electrically isolated by regions of polysilicon to produce the fingered pattern.

28. (Previously Presented) The integrated inductor of claim 24, wherein the substrate is a CMOS substrate.